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Preface

This book presents hardware and software designs for interfacing a variety of sensors to the IBM PC. It discusses each sensor and the associated electronic circuitry necessary to condition its output for interface to the PC. Examples for the use of each sensor together with a computer program that shows how to capture and use the information provided by the sensor are also included.

In this book, three different programming languages will be used for examples: BASIC, assembly language, and C. We give BASIC examples because this is the language most likely to be understood by the majority of the readers. We provide Intel 8088 assembly language examples to demonstrate use of the language that can extract the maximal performance from the computer.

We use C language examples to show the language that is the best compromise for instrumentation applications combining features of both high and low level languages. C provides a significant improvement over assembly language for implementing many applications. It is standardized and structured. Programs are based on functions that can be evolved independently of one another and put together to implement an application. These functions are to software what black boxes are to hardware. If their I/O properties are carefully specified in advance, functions can be developed by many different software designers working on different aspects of the same project. These functions can then be linked together to implement the software design of a system.

Most important of all, C programs are transportable. By design, a program developed in C on one type of processor can be transported to another. Other languages claim this capability, but C is the one that really works. Machine-specific functions such as those written in assembly language can be separated out and rewritten for a new architecture to which the program has been transported.

Many sensor systems provide analog voltage levels that must be converted to digital signals before the PC can use them. This book provides the design of a complete signal acquisition system for data conversion. Although our intent in providing this design is to unveil some of the mystery of interfacing to the system bus of the IBM PC, it also shows a practical, inexpensive, and simple design that the do-it-yourself reader can build and use. For those who require a laboratory-quality system, we provide the addresses of companies that manufacture boards that you can add to provide signal acquisition and graphics display.

This book should be useful to anyone who needs to connect any type of sensor to the IBM PC or equivalent computer. It is a particularly suitable reference for practicing electrical and computer engineers, designers, technicians, and supervisory personnel involved in or responsible for the design, installation, and operation of sensor systems. Additionally, it is particularly applicable for those who do not have a complete and intensive formal education in sensors, transducers, data conversion, and interface techniques or for those who require state-of-the-art updating in any of these areas.

Chapter 1 covers various operational amplifier circuit designs that are useful for developing the amplifiers, guards, and electronics necessary for interfacing the analog sensors. It also covers passive, active, and switched capacitor filters.

Chapter 2 gives practical information about minimizing the electrical interference in analog and digital circuit designs. It also discusses power supply considerations. These topics are frequently overlooked by designers and only considered as afterthoughts when the rest of the design is complete.

Chapter 3 explains the system bus of the IBM PC and provides the design of the basic hardware interface that supports all the other designs in the book. It also covers interrupts, counters, and timers.

Chapter 4 deals with the theory and practice of signal conversion, binary codes, sampling, and digital-to-analog converters, while Chapter 5 covers the selection and use of analog-to-digital converters.

Chapter 6 reviews the versatile serial interface available on the IBM PC and on every other microcomputer system. An example shows how to interface sensors through this interface that is normally used for connection to other devices, such as printers and modems.

Chapter 7 describes temperature sensors, such as p-n junctions, thermocouples, thermistors, and shows how to interface them.

Chapter 8 covers photon sensors for radiation, such as photoresistive, photovoltaic, and photoemissive sensors. It also covers thermal detectors such as bolometer, thermopile, and pyroelectric sensors.

Chapter 9 deals with displacement sensors, which are used to measure ac-

celeration, pressure, and displacement. It covers the potentiometric, strain gage, linear variable differential transformer, and piezoelectric sensors.

Chapter 10 describes flow sensors, including thermal, mechanical, differential pressure, electromagnetic, and ultrasonic types.

Chapter 11 explains the basics of operation of many of the familiar microcomputer interface devices and shows how to interface them to the PC. It includes such devices as the joystick, trackball, mouse, x-y digitizer, light pen, and digital camera.

Chapter 12 presents the use of the standardized general purpose interface bus (GPIB) with a PC. This is an approach for controlling and accessing multiple instruments, each with its own sensor or controller interface.

Chapter 13 describes techniques for telecommunication of acquired data among computers. It discusses the use of modems for communication by telephone. This is important for remote sensing applications where a central computer is separated by a large distance from a computer acting as a sensing system.

Chapter 14 discusses the concept of the local area network (LAN) that is becoming increasingly important, particularly for business applications. The LAN provides a way to interconnect sensing systems in a restricted physical environment, such as in a group of laboratories.

Appendix A provides the names, addresses, and telephone numbers of manufacturers of data acquisition systems and other hardware designed for use with the IBM PC.

Appendix B gives the port assignments for the prototype board designed in this book and also for the Tecmar Lab Master data acquisition system used in examples throughout the book.

Appendix C provides the complete software listing for a digital oscilloscope program for the IBM PC. This program uses the prototype board developed in this book for signal acquisition and the Hercules graphics board for display. For this high-performance application, the program is developed in the C language.

We assume a general technical background in the reader so that the circuit and software may be readily understood.

WILLIS J. TOMPKIN
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1

Amplifiers

Gordon T. Geheb and Janet Nack

Transducers convert physical variables being measured to electrical outputs. In this book sensors (input transducers) that detect a variety of physical variables, such as temperature, pressure, flow, and motion, are discussed. A sensor then supplies its electrical output signal to signal-conditioning circuitry, which prepares it for interfacing to the IBM PC. The output of the sensor is usually quite small and requires amplification. An amplifier not only provides gain but may also provide filtering, signal processing, or correction for nonlinearities. In this chapter we emphasize the operational amplifier (op amp) because of its ease of use in circuit design compared to discrete transistor circuits.

1.1 IDEAL OP AMPS*

An op amp is a high-gain direct-current (dc) differential amplifier. It is normally used in circuit configurations that have characteristics determined by external feedback networks.

The transfer function of an electronic circuit is the ratio of the output function to the input function. For a voltage amplifier the transfer function (gain)

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* Section 1.1 written by Gordon T. Geheb.

is

$$A_v = \frac{v_o}{v_i} \tag{1.1}$$

The best approach in circuit design is first to assume that the op amp is ideal, which makes calculation of the transfer function much easier. After the initial design, we check the nonideal characteristics of the op amp to determine their effect on the circuit. If the effects are not important, the design is complete; otherwise, additional design is needed.

Figure 1.1 shows a simplified op-amp equivalent circuit. The model consists of an input impedance R_d connected between the two input terminals v_1 and v_2. The output circuit consists of a controlled-voltage source in series with an output resistance R_o connected to the output terminal. A voltage difference between the two input terminals causes a current flow through R_d. The differential voltage is multiplied by A, the gain of the op amp, to generate the output voltage.
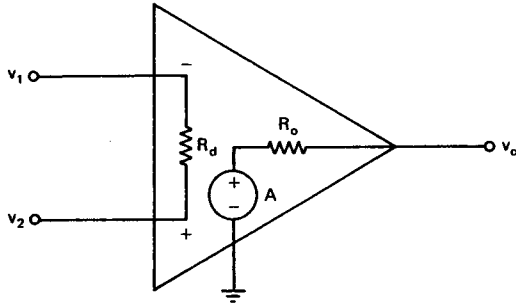
Figure 1.1 Op-amp equivalent circuit.

To simplify design calculations, the following characteristics are assumed for an ideal op amp (Carr, 1976):

1. Open-loop gain = infinity
2. Input impedance R_d = infinity
3. Output impedance R_o = 0
4. Bandwidth = infinity (infinite frequency response)
5. v_o = 0 when v_1 = v_2 (no offset voltage)

This last characteristic is very important. Figure 1.1 shows $v_2 - v_1 = v_o/A$. If v_o is finite and A is infinite (typically 100,000), then $v_2 - v_1 = 0$ and $v_1 = v_2$. Since R_d, the differential impedance between v_1 and v_2, is large and $v_1 = v_2$, we can usually neglect the current in R_d (Shilling and Belove, 1979). These two assumptions are very helpful in designing op-amp circuits; we summarize them as follows:

Rule 1. When the op amp is in the linear range the two inputs are at the same voltage.

Rule 2. No current flows into either terminal of the op amp.

When op amps are shown in circuit diagrams, the triangular symbol of Figure 1.1 is shown, but the internal elements are not.

1.2 BASIC OP-AMP CIRCUIT BLOCKS*

In the following sections we assume that the op amp is ideal and obtain a number of useful circuits. In most circuits, op amps are used in closed-loop configurations. Feedback networks around the op amp reduce the gain and provide other useful features.

Inverting Amplifier

Figure 1.2 shows the basic inverter circuit. It is used in a variety of applications, including instrumentation. The feedback impedance, in this case R_f, provides the inverting amplifier with many advantages, such as increased bandwidth and lower output impedance.
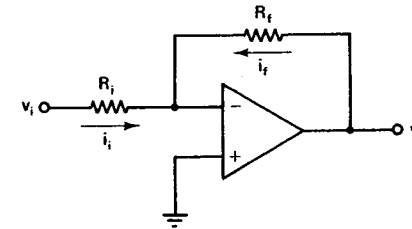
Figure 1.2 The basic inverter circuit has a gain equal to $-R_f/R_i$.

Gain equation. We can easily calculate the gain equation (transfer function) for this circuit. Since the noninverting input is grounded, it is at a potential of 0 V. By rule 1 the inverting input is also at a potential of 0 V, and is called a virtual ground. The inverting terminal in Figure 1.2 is therefore grounded for all practical purposes.

Kirchhoff's current law says that the sum of all currents entering and leaving a junction must be zero. By rule 2 no current flows into the input of the op amp; therefore, $i_i + i_f = 0$ and

$$i_i = -i_f \tag{1.2}$$

Since the right side of R_i is at ground potential (0 V), and the left side is v_i, then by Ohm's law $i_i = v_i/R_i$. Using the same reasoning, $i_f = v_o/R_f$. Substitution of these equations into Eq. (1.2) yields

$$\frac{v_i}{R_i} = \frac{-v_o}{R_f} \Rightarrow \frac{v_o}{v_i} = \frac{-R_f}{R_i}. \tag{1.3}$$

* Section 1.2 written by Gordon T. Geheb.

The circuit, therefore, inverts the input signal, and the inverting amplifier gain is $-R_f/R_i$.

Input/output characteristics. The linear range of the circuit is determined by the power-supply voltages. Figure 1.3 shows that the circuit saturates for a ± 15-V power supply when v_o exceeds V_s, the saturation voltage, which is typically ± 13 V. Any increase in v_i results in no change in the output. For most op amps the maximal linear output voltage swing is about 4 V less than the difference in power-supply voltages (Webster, 1978).
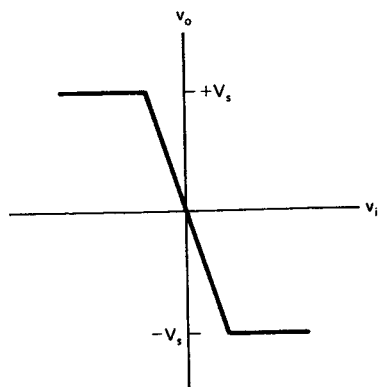
Figure 1.3 The inverter input/output characteristics are linear only up to the saturation voltage V_s.

The input impedance of the inverting amplifier is usually quite low. Because the inverting terminal is essentially grounded, the input impedance seen by the signal is R_i. By increasing R_i, the input impedance can be increased, but this decreases available gain. The gain can be increased by increasing R_f, but there is a practical limit to the maximal value of R_f.

Noninverting Amplifiers

Figure 1.4 shows the second basic op-amp circuit, the noninverting amplifier. By rule 1, v_i also exists at the inverting input of the op amp. By rule 2, i_f must flow through R_i to ground since no current can flow into the op amp. By the voltage-divider rule,

$$v_i = \frac{R_i v_o}{R_i + R_f} \qquad (1.4)$$

$$\frac{v_o}{v_i} = \frac{R_i + R_f}{R_i} = 1 + \frac{R_f}{R_i}$$

In the noninverting amplifier the circuit gain is positive and is always greater than or equal to 1, and the input impedance is very large, approximately infinity (Jung, 1981).
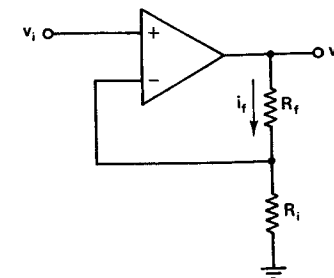
Figure 1.4 The noninverting amplifier circuit has a gain of $(R_f + R_i)/R_i$.

Unity-Gain Amplifier

In the noninverting amplifier, if we set R_i equal to infinity and R_f equal to zero, the circuit reduces to Figure 1.5. By rule 1, v_i must also exist at the inverting input, which is connected directly to v_o. Therefore, $v_o = v_i$ and the output voltage follows the input voltage.
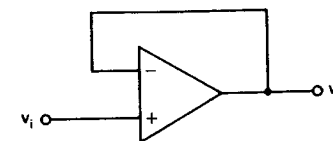
Figure 1.5 The unity-gain amplifier has very high input impedance.

One question might be: Why have a gain of 1? A very important answer is that the unity-gain amplifier is useful as a buffer amplifier or as an impedance converter. As a buffer amplifier the unity-gain amplifier isolates one circuit from the loading effects of a following stage. One application is in data conversion systems. Many analog-to-digital converter circuits have a varying input impedance over the analog input-signal voltage range. With a unity-gain amplifier we achieve a constant input impedance. For some digital-to-analog converters we need a high-impedance load for correct operation but do not desire output voltage scaling. The unity-gain amplifier is needed in this application. It is also useful following the hold capacitor in a sample-and-hold circuit to prevent capacitor discharge during conversion time.

Differential Amplifiers

A very important op-amp configuration is the differential amplifier, a combination of the inverting and noninverting configurations that has unique characteristics of its own. When amplifying bioelectric signals from ECGs and EEGs, the differential amplifier can reject 60-Hz interference, which is common to both inputs of the amplifier (Tompkins and Webster, 1981).

Figure 1.6(b) shows a simple one-op-amp differential amplifier. By rule 2, no current flows into the op-amp inputs, so current flows from v_2 through R_1
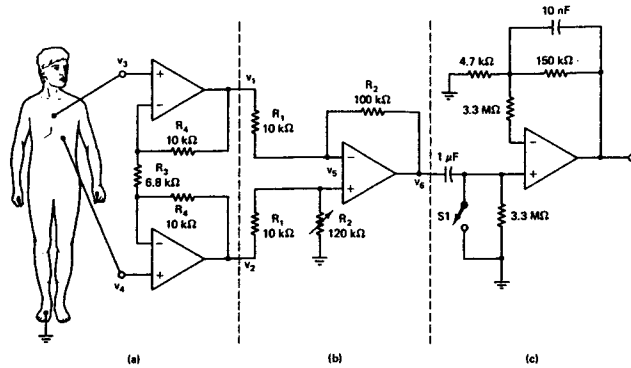
Figure 1.6 Electrocardiogram amplifier. (a) and (b) Instrumentation amplifier stage. (c) Noninverting amplifier stage.

and R_2 to ground. Thus by the voltage-divider rule the voltage at the noninverting input is

$$v_5 = \frac{R_2 v_2}{R_1 + R_2} \tag{1.5}$$

By rule 1 the voltage at the inverting input must equal the voltage at the noninverting input. Therefore, the top half of the circuit acts as an inverter. Solving for the current in the top half of the circuit as done for the inverter yields

$$i = \frac{v_1 - v_5}{R_1} = \frac{v_5 - v_6}{R_2} \tag{1.6}$$

Substitution of Eq. (1.5) into Eq. (1.6) yields

$$v_6 = \frac{(v_2 - v_1)R_2}{R_1} \tag{1.7}$$

which is the gain equation of the differential amplifier. The equation for the differential amplifier shows that if the two inputs are tied together and driven by the same voltage source so that the common-mode voltage (CMV) is $v_1 = v_2$, then $v_6 = 0$. The term "common mode" is used because both inputs have a common driving voltage. The common-mode gain (CMG) of the differential amplifier circuit is 0.

If $v_1 \neq v_2$, then the differential voltage gain (DG) is equal to R_2/R_1. In practice the differential amplifier cannot perfectly reject the common-mode voltage. A quantitative measure of the ability of the differential amplifier to reject common-mode voltage is called the common-mode rejection ratio (CMRR):

$$CMRR = \frac{DG}{CMG} \tag{1.8}$$

The CMRR may range from 100 in some applications to greater than 10,000 for high-quality biopotential amplifiers. The differential amplifier configuration is

unique because it can reject a signal such as 60-Hz noise that is common to both inputs.

Instrumentation Amplifiers

The one-op-amp differential amplifier has a low input impedance which is satisfactory for low-impedance sources, such as strain-gage bridges. However, it is not satisfactory for high-impedance sources. A solution to this is the instrumentation amplifier shown in Figure 1.6(a) and (b). It has a noninverting amplifier connected to each of the inputs of the basic differential amplifier. The R_i's of the noninverting amplifiers are connected together, which eliminates the connection to ground. The common-mode gain is determined by considering the two followers separately from the simple differential amplifier. Assume that $v_3 = v_4$; by rule 1, v_3 appears at the inverting inputs of both op amps. This puts the same voltage at both ends of R_3, and thus no current flows through R_3. By rule 2, current flowing out of the input terminals of the op amp is zero, so no current flows through the R_4's. Voltage v_3 appears at both op-amp outputs and the CMG is 1.

To determine the differential gain we assume that $v_3 \neq v_4$. The resistor R_3 then has a voltage drop across it equal to $v_3 - v_4$. This causes a current to flow through R_3, and by rule 2 the same current also flows through both R_4's. The output voltage is

$$v_1 - v_2 = i(R_4 + R_3 + R_4) \tag{1.9}$$

while the input voltage is

$$v_3 - v_4 = iR_3 \tag{1.10}$$

The differential gain is then

$$DG = \frac{v_1 - v_2}{v_3 - v_4} = \frac{2R_4 + R_3}{R_3} \tag{1.11}$$

The CMRR is determined by the DG since the CMG is 1. Since the CMG of the first stage of the instrumentation amplifier equals 1, the overall CMG is zero because the inputs to the second stage are equal.

Multiplying the gains of each stage [Eqs. (1.11) and (1.7)] yields the overall gain of the instrumentation amplifier:

$$v_6 = (v_3 - v_4)\frac{R_2}{R_1}\frac{2R_4 + R_3}{R_3} \tag{1.12}$$

It has high input impedance, high CMRR, and a gain that is adjustable by changing R_3. This circuit rejects the 60-Hz interference that is common to both inputs of the instrumentation amplifier (Webster, 1978).

The Electrocardiogram Amplifier

An example of the use of the instrumentation amplifier is the electrocardiogram (ECG) amplifier. The instrumentation amplifier's ability to reject interference makes it a good choice for the preamplifier stage of a multiple op-amp circuit.

Since it has high interference immunity, only the desired signal is amplified through the remaining stages of the amplifier. The high input impedance provided by this amplifier is desirable because it represents the load seen by the ECG electrodes.

Figure 1.6 is an ECG amplifier. The instrumentation amplifier provides high input impedance and high CMRR. The 120-kΩ potentiometer permits maximization of the CMRR. Since electrodes may produce an offset potential of up to 0.2 V (Webster, 1978), the gain of the dc-coupled preamplifier stage (instrumentation amplifier stage) is intentionally low to prevent saturation. From Eq. (1.12), the gain is 40. No coupling capacitors are used at the input because they would block the op-amp bias current. The 1-μF coupling capacitor and the 3.3-MΩ resistor form a high-pass filter. As calculated from the transfer function of the simple high-pass filter, the filter passes frequencies above 0.05 Hz. The output stage is a noninverting amplifier with a gain of approximately 32 [Eq. (1.4)]. The 10-nF capacitor and the 150-kΩ resistor produce a low-pass filter which passes frequencies up to 100 Hz. The 3.3-MΩ resistor at the inverting input balances bias-current source impedances (Section 1.5). When the output saturates, S_1 may be momentarily closed in order to charge the 1-μF capacitor. This is done after lead switching or defibrillation to return the output to the linear region. Popular 741 op amps work well in this circuit, but op amps with low bias current may be desired to keep dc current through the electrodes small.

1.3 ANALOG COMPUTATION*

Op-amp circuits can perform analog computation and other mathematical operations. However, the tendency is toward using digital signal processing because of its flexibility and elimination of hardware. Analog signal processing may have advantages when digital processing consumes too much time.

Inverters and Scale Changers

Many times, signal inversion or voltage scaling is desired. The inverting amplifier configuration can provide desired gain changes and sign inversion with the proper choice of R_f/R_i. One possible application is use of the inverter to scale the output of a digital-to-analog converter.

Adders (Summing Amplifiers)

The inverter can sum several input voltages. Each input connects to the inverting input through a weighting resistor. The inverting input is called a summing junction because this node sums all input and feedback currents.

Figure 1.7 shows the basic summing amplifier. As in the inverting amplifier the voltage at the inverting input must equal zero, and therefore the current

* Section 1.3 written by Gordon T. Geheb.
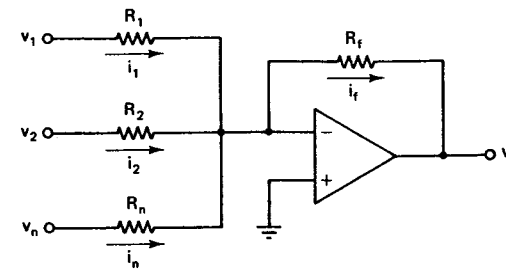
Figure 1.7   Basic summing amplifier.

flowing into the op amp equals zero. Thus

$$i_f = i_1 + i_2 + \ldots + i_n$$

and

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad \ldots, \quad i_n = \frac{v_n}{R_n} \qquad (1.13)$$

Since the inverting input is at zero voltage, $v_o = -i_f R_f$, thus by substitution,

$$v_o = -R_f \left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \ldots + \frac{v_n}{R_n} \right) \qquad (1.14)$$

Resistor R_f determines the overall gain of the circuit. The resistances R_1, R_2, $\ldots$, R_n determine the weighting factors and input impedances of the respective channels.

The circuits discussed previously contained primarily resistive elements. The inverting amplifier can be further modified by using capacitors. The same basic ideal characteristics are used in the analysis.

Integrators

The integrator is an electronic circuit that produces an output proportional to the integral of the input signal. Figure 1.8 shows a simple analog integrator. Capacitor C has one terminal at the summing junction and the other at the output. Therefore, the capacitor voltage is also the output voltage. We cannot describe the integrator output by a simple algebraic relation because for a fixed input the output changes at a rate determined by v_i, R, and C. Thus we must know how long an input has been applied to determine the output voltage. The

Figure 1.8   Simple analog integrator.

voltage across an initially uncharged capacitor is

$$v = \frac{i_f t_1}{C} \tag{1.15}$$

where i_f is the current through C and t_1 is the duration of integration. For v_i positive, $i_i = v_i/R$. Since $i_f = i_i$ and due to inversion,

$$v_o = \frac{-1}{RC} \int_0^{t_1} v_i \, dt + v_{ic} \tag{1.16}$$

This shows that v_o is equal to the negative integral of the input voltage over the time from 0 to t_1 scaled by the gain factor of $1/RC$. The voltage v_{ic} is the initial-condition voltage of the capacitor.
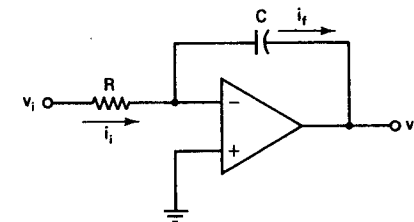
The idealized integrator of Figure 1.8 has a serious drawback; if v_i is left connected indefinitely, v_o will decrease until it reaches the saturation voltage of the op amp. This occurs because the integrator operates as an open-loop amplifier for dc inputs (Webster, 1978). Figure 1.9(a) shows a practical integrator that prevents this problem. During the reset cycle, S_1 is closed and S_2 is open. The circuit functions as an inverter that charges C to $-v_{ic}$, an inverted multiple of the reference voltage V_r. Since the input resistance equals the feedback resistance, the inverter gain is -1, v_o equals V_r, and C is initialized to V_r. During the integration cycle, S_1 is open and S_2 is closed. During the hold cycle, both switches are open, which keeps the output voltage v_o constant for readout and subsequent processing.
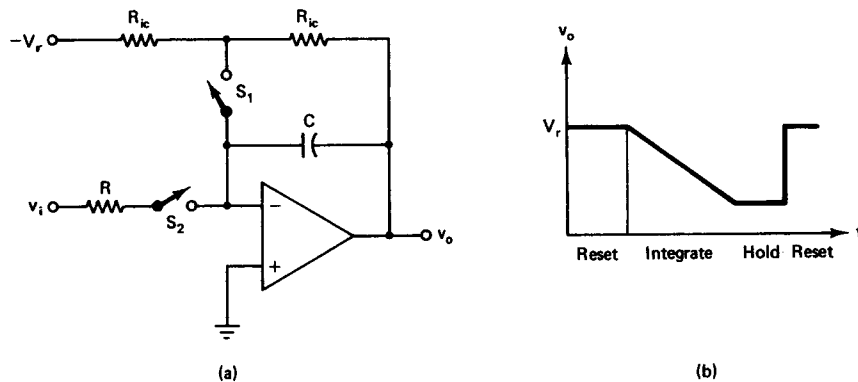
Figure 1.9 Practical integrator circuit.

Switches S_1 and S_2 can be relay contacts or solid-state switches such as FETs (field-effect transistors) or analog switches (Tompkins and Webster, 1981). External logic controls the switching. This simplifies setting initial conditions and initiating integration when several integrators are used in the solution of a differential equation. Figure 1.9(b) shows the operating sequence.

Differentiators

The differentiator gives an output signal proportional to the time rate of change of the input signal (Carr, 1976). Figure 1.10 shows a simple differentiator circuit. The current through the capacitor is

$$i_i = C \frac{dv_i}{dt}$$

If dv_i/dt is positive, i_i flows through R in a direction such that it yields a negative v_o. Thus

$$v_o = -RC \frac{dv_i}{dt} \tag{1.17}$$
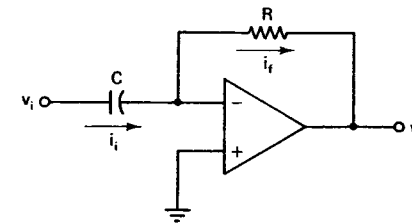
Figure 1.10 Simple differentiator circuit.

This method of differentiation seems simple, but practical differentiation gives rise to stability problems at high frequencies (Jung, 1981). The instability of the circuit is due to the intersection of the ideal gain curve of the differentiator with the open-loop gain curve of the op amp, which is shown in Figure 1.11(b). In Figure 1.11(a) R_i is added to make the gain curve of the differentiator bend over at the point where the curves intersect, $f_i = 1/(2\pi R_i C)$. R_i spoils the differentiator at high frequencies. The intersection can be shown to occur at the frequency $\omega_i^2 = A_0\omega_0/RC$ (Scidmore, 1983). From this and equation $R_i C =$
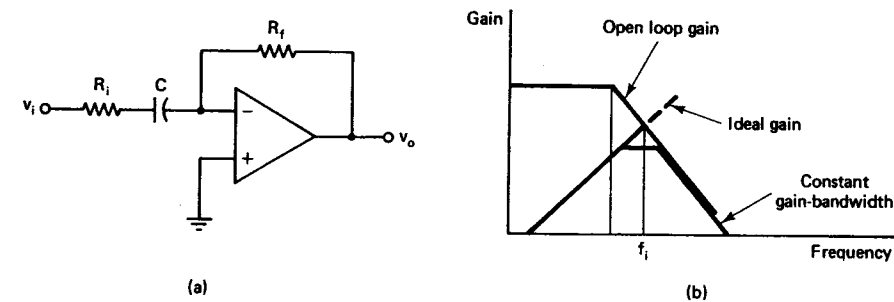
Figure 1.11 Practical differentiator. (a) Circuit diagram. (b) Gain-vs-frequency characteristics.

$1/\omega_i$, we find that for design of a stable circuit

$$\omega_i = \left(\frac{A_0\omega_0}{RC}\right)^{1/2} = \frac{1}{R_iC} \qquad (1.18)$$

or

$$R_i = \left(\frac{R}{A_0\omega_0C}\right)^{1/2} \qquad (1.19)$$

$A_0\omega_0$ is the gain–bandwidth product of the op amp.

Some op amps are better suited than others for differentiator use. The high-frequency characteristics tend to limit the choices to devices with high slew rate and gain–bandwidth product. A high-slew-rate FET op amp, such as the LU356, is a good choice for differentiator applications.

1.4 NONLINEAR OP-AMP APPLICATIONS*

Comparators

A comparator is a circuit that compares two input voltages and produces an output relative to the state of the two input terminals (Webster, 1978). Figure 1.12(a) shows a basic comparator circuit. Because there is no feedback impedance, the op amp operates open loop. One input is set as a reference potential and the other is the unknown input. The comparator output indicates whether the unknown input signal is above or below the reference voltage. In Figure 1.12(a) the reference voltage V_r is fed to the noninverting input while v_i is applied to the inverting input. When v_i becomes greater than V_r the output v_o becomes $-V_s$ (the negative saturation voltage). For v_i less than V_r, $v_o = +V_s$. We may interchange the inputs to invert the output. Figure 1.12(b) shows the transfer characteristic.

A comparator should change output states as quickly as possible. The comparator operates open loop, so there is no necessity for frequency compensation (Section 1.5) since there is no closed loop to stabilize. Frequency compensation slows down the speed, response time, and slew rate. Response time is the time required for an output transition to occur once an input trigger has arrived. Slew rate indicates how quickly the amplifier output can change during a transition. The National Semiconductor LM101A op amp is good for comparator applications because of its high slew rate.

Comparators with Hysteresis

For the simple comparator of Figure 1.12, if there is noise on v_i, v_o will fluctuate very rapidly between $\pm V_s$. A solution to this problem is the introduction of positive feedback around the comparator (done by feeding part of the output

* Section 1.4 written by Gordon T. Geheb.

(a)   (b)
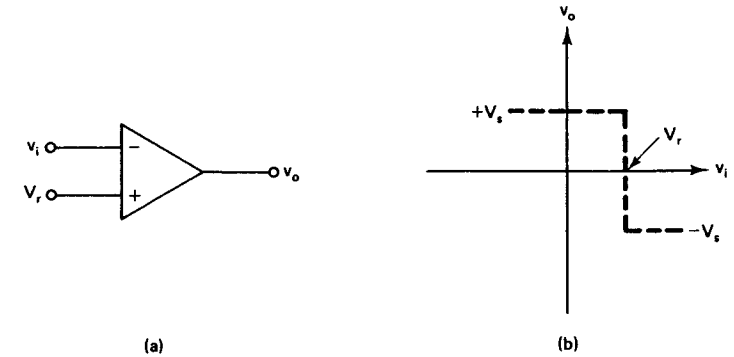
Figure 1.12 Simple comparator. (a) Circuit diagram. (b) Transfer characteristics.

signal back to the noninverting input) (Jung, 1981). Figure 1.13(a) shows a circuit for a comparator with hysteresis. By introducing R_2, positive feedback is developed across R_1. If the output is high, R_2 feeds back a signal which is added to the reference voltage. The increase in V_r is

$$\Delta V_r = \frac{(V_s - V_r)R_1}{R_1 + R_2} \qquad (1.20)$$

Thus the reference voltage is increased:

$$V_{r+} = V_r + \Delta V_r \qquad (1.21)$$

Therefore, a new transition voltage is introduced which is higher than V_r by the amount of positive voltage feedback from v_o. As v_i crosses above $V_r + \Delta V_r$ the output starts to fall, and as the falling condition is sensed across R_1 the noninverting

(a)   (b)
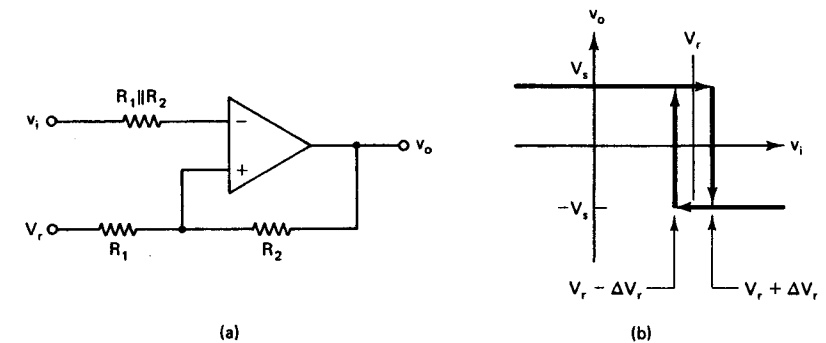
Figure 1.13 Comparator with hysteresis. (a) Circuit diagram. (b) Transfer characteristics.

input is also driven negative. Because the positive feedback is regenerative the output quickly falls to the opposite state. Since v_o is now at $-V_s$ the voltage fed back is

$$\Delta V_r = \frac{(-V_s - V_r)R_1}{R_1 + R_2} \tag{1.22}$$

making a new negative reference voltage:

$$V_{r-} = V_r - \Delta V_r \tag{1.23}$$

The transfer characteristics shown in Figure 1.13(b) illustrate the effect of the hysteresis loop. With the addition of the positive feedback, noise on v_i cannot cause v_o to flip back and forth to $\pm V_s$. For example, if v_i has gone above $V_r + \Delta V_r$ and v_o has just flipped to $-V_s$, v_i must fall below $V_r - \Delta V_r$ before it will flip back to its original state. The width of the hysteresis can be varied by using a potentiometer in place of R_1.

Rectifiers

Simple resistor–diode rectifiers do not function well for voltages below 0.7 V because the forward voltage drop of the diode cannot be overcome. Placing the diode within the feedback loop of an op amp cures this problem because the gain of the op amp reduces the voltage limitation.

Precision half-wave rectifiers. Figure 1.14 shows a half-wave rectifier circuit that produces an inverted half-wave replica of the input signal. When v_i is negative, D_1 is forward biased, D_2 is reverse biased, and the circuit acts as a regular unity-gain amplifier. For v_i positive, D_1 is nonconducting and D_2 is conducting, which applies negative feedback and locks the output at the reverse-biased voltage of the diode. If diode D_2 were not used, the output voltage would clamp to $-V_s$. However, v_o would still equal 0 V.
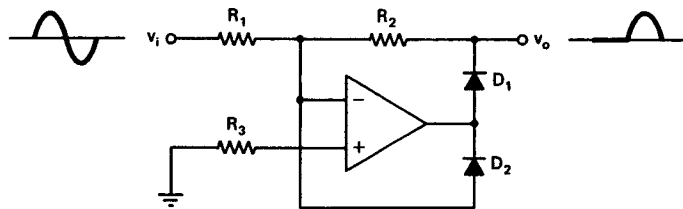

Figure 1.14   Precision half-wave rectifier.

Precision full-wave rectifiers. Figure 1.15 shows a circuit for a full-wave precision rectifier. When v_i is greater than zero, the input signal is fed directly through the feedback network to the output. Since the input signal is positive, it drives the output terminal of the inverting amplifier negative. The diode,
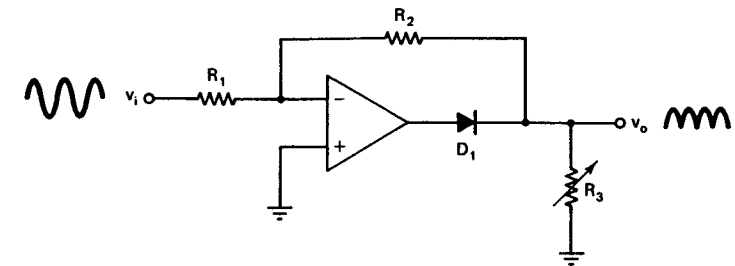
Figure 1.15   Precision full-wave rectifier.

therefore, does not conduct and the op amp is disconnected from the signal path. During a negative input signal the circuit acts as a normal inverting amplifier with a gain equal to $-R_2/R_1$. The potentiometer can be adjusted to make the full-wave output symmetrical.

Limiters

In many applications we must limit the output. It is best to do this limiting before the amplifier reaches the saturation voltage because the amplifier requires a long recovery time when saturated before it can operate linearly again (Jung, 1981). In digital logic circuits, the positive or negative limit required for operation is usually much lower (5 V) than the typical op-amp voltage swing (± 13 V). A limiter circuit is a good choice for this reduction.

Figure 1.16 shows a feedback limiter that uses a zener diode as the feedback impedance of an inverter. The values of the zener forward and reverse voltages establish the limits of the output voltage. If v_i is negative, the output of the op amp is positive and the zener diode is reverse biased. This drives it into the breakdown region and fixes the output voltage at V_z. For positive input voltages the output of the op amp goes negative. This forward biases the zener diode, which sets the output limit equal to the forward voltage drop of the zener diode (typically 0.7 V).

Figure 1.16   Limiter circuit.

The output voltage is equal to that of the diode used and may be inverted by reversing the zener diode.

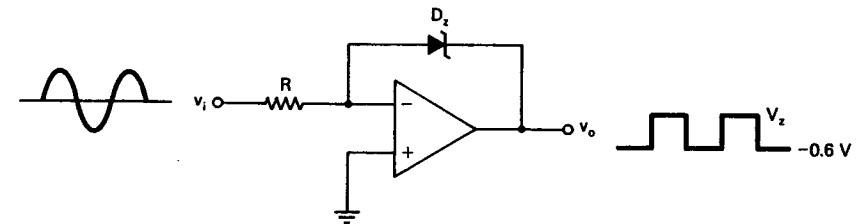## 1.5 OP-AMP CONSIDERATIONS*

In the preceding sections we assumed an ideal op amp. Now we consider the effects of some nonideal characteristics.

Compensation

Since the op amp must have high gain, it has several internal stages. Each stage has stray capacitance that limits its high-frequency response. At high frequencies undesirable oscillation may arise because the circuit phase shift may become greater than $-180°$ when the loop gain equals 1 (the closed-loop condition for oscillation). Adding an external capacitor to the terminals shown on the op-amp specification sheet moves one of the internal RC filter corner frequencies to a low frequency. This compensates the uncompensated op amp and ensures a maximal phase shift of less than $-180°$. The 741 has this compensation added internally, and therefore does not oscillate for any of the configurations discussed (Webster, 1978).

Gain–Bandwidth Product

The gain–bandwidth product of the op amp is equal to the product of gain and bandwidth at a particular frequency. Along the entire straight line shown in Figure 1.11(b), the gain–bandwidth product is constant (typically, 1 MHz). Thus, for a noninverting amplifier circuit, we can obtain the bandwidth by dividing the gain–bandwidth product by the amplifier circuit gain.

Input Offset Voltage

The ideal op amp has the property of zero output voltage when the input voltage is zero. Practical op amps do not exhibit this feature; they have an input offset voltage. The input offset voltage is the voltage that must be applied between the two input terminals to obtain zero output voltage. Each op-amp input drives a transistor. If the base-to-emitter voltage drop is different for each op amp, then in order to have $v_o = 0$ the voltage $(v_1 - v_2)$ must have a value on the order of millivolts. The offset voltage is not usually important when the input voltage is larger than 1 V. When amplifying small signals as in the case of sensors, the offset voltage may be important.

The offset voltage is nulled by introducing an opposing voltage at one of the op-amp terminals. This is done by adding an external potentiometer to the terminals shown on the specification sheet, which increases current through one of the transistors and lowers the current through the other.

Input Bias Current

In practical op amps, the current flowing into the terminals is not zero. In order to keep the input transistor of the op amp turned on, a base or gate current called the input bias current must flow all the time. When this current flows

* Section 1.5 written by Gordon T. Geheb.

through the feedback network it causes errors proportional to the feedback network resistances. To minimize these errors, feedback resistors should be kept low, such as below 10 kΩ.

Since the difference between the two input bias currents is much smaller than either of the bias currents alone, we can achieve a cancellation effect by having each current flow through the same resistor. We accomplish this by connecting a resistor having the value of the parallel combination of R_i and R_f in series with the positive input of the op amp. There still is error but it is now determined by the difference in bias current.

Slew Rate

Slew rate is the maximal rate of change of the amplifier output voltage. When rapid changes are demanded in the output, the current available to charge and discharge the compensation capacitor is limited and slew-rate limiting occurs (Shilling and Belove, 1979). For example, the 741 has a slew rate of 0.5 V/μs. Thus the output cannot change from -5 V to $+5$ V in less than 20 μs. To minimize slew-rate problems we can use an op amp for which we can select a smaller external compensating capacitor.

Power Supply

The usual supply voltages are ± 15 V. When v_o is allowed to exceed the op-amp biasing voltages the op amp will saturate and is said to be out of the amplifier's linear range (typically ± 13 V). We may reduce the power-supply voltage, but this also reduces the linear range. When the power supply goes below approximately 4 V the internal biasing voltages of the device are not satisfied.

It would be convenient always to have dual-polarity power supplies available in equipment or circuits using op amps. Unfortunately, this is not possible. There are, however, certain circuitry tactics for using the operational amplifier in single-polarity configurations. One solution is to ground the minus supply terminal, while the positive is connected to V_{cc} in the usual way. Figure 1.17
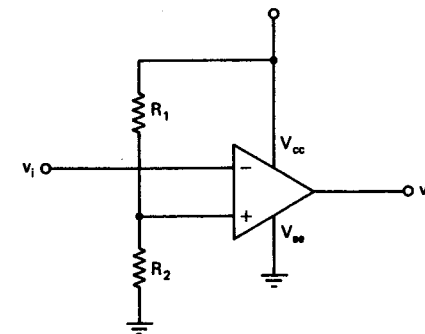

Figure 1.17 Single power-supply circuit.

shows this circuit. The noninverting input is connected to a junction on a voltage-divider network. This effectively raises the operating point above ground.

Different Op Amps

Op amps are bipolar or FET types. The bipolar op amps have a pair of bipolar input transistors. They have good input offset voltage stability but moderate input bias currents and input resistances. FET-input op amps with a pair of input FETs offer very low input bias currents and very high input resistances but have poor input offset voltage stability (Dostal, 1981).

Programmable Op Amps

A programmable op amp such as the UC4250 permits setting the power consumption and dynamic properties of the op amp. By adding the proper external resistor, we can adjust the quiescent supply current [the operating current flowing in a circuit during zero-signal (idle) intervals]. Lower quiescent currents yield lower frequency responses and lower output current capabilities (Dostal, 1981).

Common Op Amps

Figure 1.18 shows characteristics of commonly used op amps.

Type	Feature	Input bias current	Offset voltage	GBW	Price
741	Low cost	80 nA	2 mV	1 MHz	$0.35
308	Low bias current	3 nA	2 mV	1 MHz	0.69
ICL8007	FET input	50 pA	50 mV	1 MHz	5.00
CA3130	FET input	6 pA	20 mV	4 MHz	0.89
OP-07	Low offset	1 nA	30 μV	800 kHz	1.99
LH0052	Low offset	0.5 pA	0.1 μV	1 MHz	5.00
LF351	High GBW	50 pA	5 mV	4 MHz	0.62
LM312	Low bias current	3 nA	0.7 mV	1 MHz	2.49
UC4250	Programmable	7.5 nA	4 mV	800 kHz	1.84

Figure 1.18 Common op amps, typical specifications, and 1986 prices.

1.6 GUARDING*

Guarding exploits the fact that no current flows through an electrical component having both its terminals at the same voltage. Guarding is a term that is used in two different contexts; it is a technique used to eliminate surface leakage currents or to eliminate common-mode signals.

* Section 1.6 written by Janet Nack.

Elimination of Surface Leakage Currents

To eliminate surface leakage currents, guarding is accomplished by surrounding the input leads with a conductor, which is supplied by a low-impedance voltage source. By maintaining the guard at the same voltage as the input leads, leakage currents are drastically reduced. The best example of this is the coaxial cable with a grounded shield shown in Figure 1.19(a). Without the guard connection, there is considerable leakage current from the central conductor through the cable insulation to ground. Figure 1.19(b) shows that this results in an attenuated output voltage. However, with the guard connection shown in Figure 1.19(c), the leakage current is negligible (Keithley, 1984) (Strong, 1970).

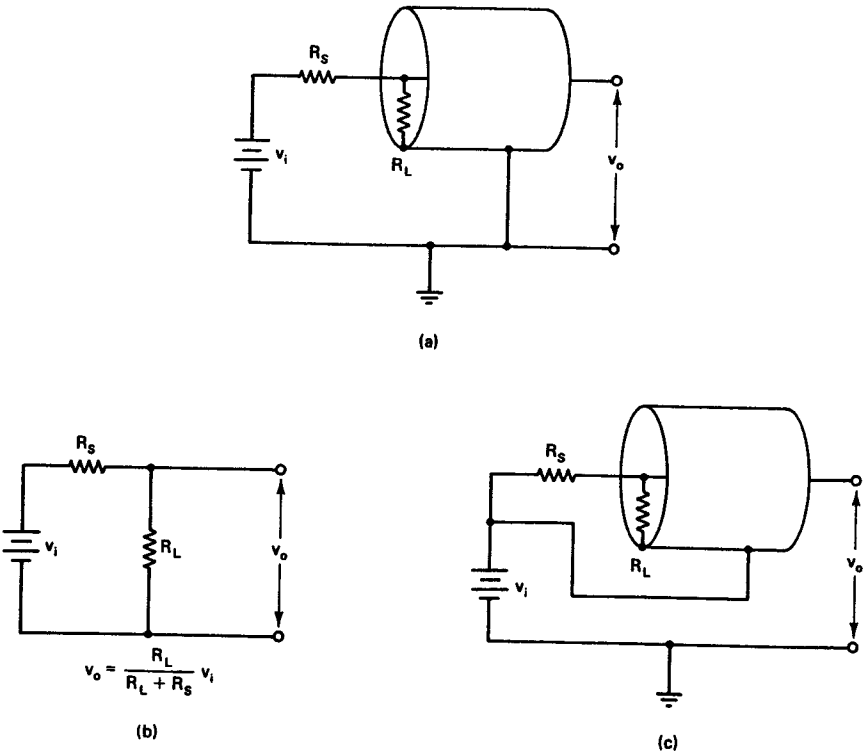(a)

$$v_o = \frac{R_L}{R_L + R_s} v_i$$

(b)

(c)

Figure 1.19 (a) Grounded coaxial cable. (b) Equivalent circuit. (c) Guarded coaxial cable.

Figure 1.20 shows guarding applied to an ionization chamber. When measuring ionization currents (10 pA), leakage currents must be smaller than 10 fA or errors
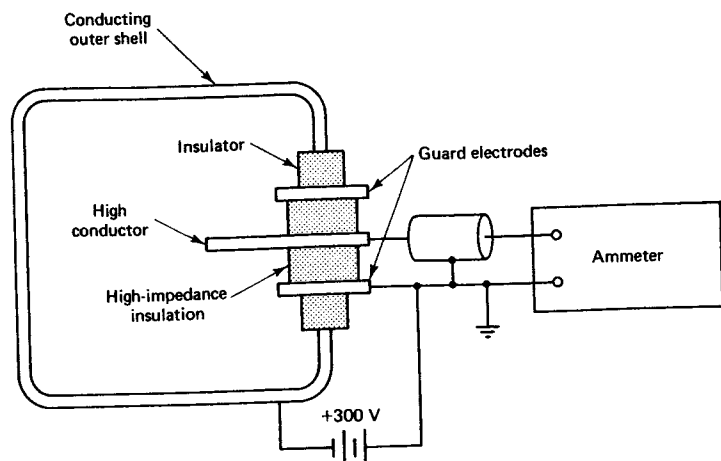
Figure 1.20   Guarded ionization chamber. (From G. F. Knoll, *Radiation detection and measurement*, Wiley, New York, 1979.)
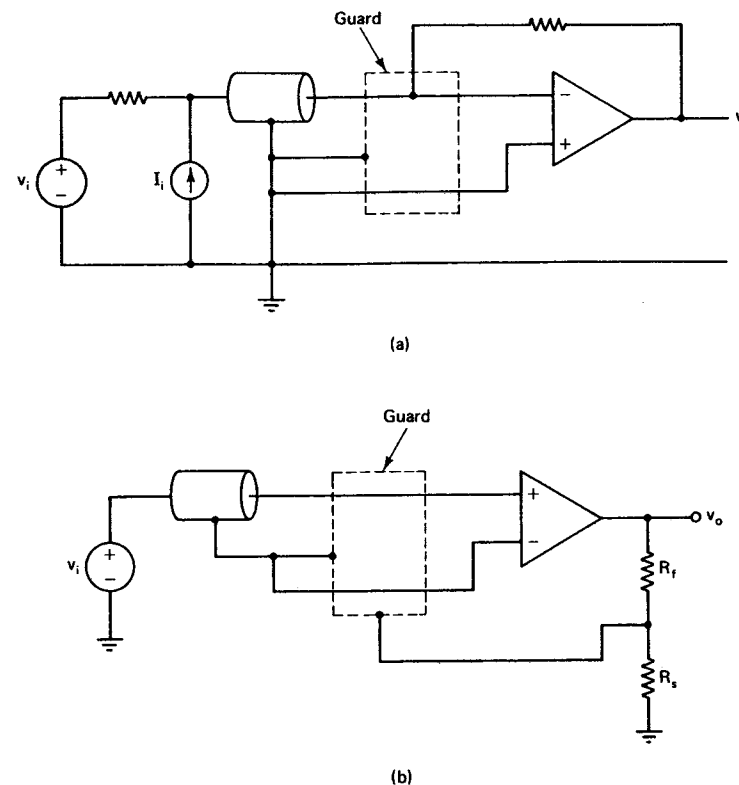

(a)

(b)

Figure 1.21   Guarded inputs for (a) inverting, and (b) noninverting amplifiers. The dashed line shows that the guard ring on the circuit board surrounds the amplifier input terminals. (From Analog Devices, Data acquisition components and subsystems, Norwood, MA, 1980.)

occur. When a large voltage is applied, the insulator must have an extremely high resistance in order to keep leakage currents small. The solution to this problem is the division of each insulator by a guard conductor. Now the majority of the voltage drop occurs across the outer insulation, and the voltage difference between the HI conductor and the guard conductor is reduced to the small voltage drop between the terminals of the ammeter. This reduces the measured leakage current (Keithley, 1984).

The main application of this technique is the guarding of amplifier inputs. In order to realize the low input current characteristics desired by users of amplifiers, we must eliminate leakage currents. This is accomplished by applying a voltage to a shield on the outside of the insulating material surrounding the a voltage to a shield on the outside of the insulating material surrounding the high-impedance input lines. Because this voltage is equal to that of the high-high-impedance input lines. Because this voltage is equal to that of the high-impedance input lines, there is no voltage drop across the insulation; therefore, impedance input lines, there is no voltage drop across the insulation; therefore, the leakage current is eliminated. This technique provides the user with additional benefits as well. It reduces interference pickup and the effective capacitance between the guard and the central conductor. The case of the amplifier, if not grounded, may also be connected to the guard voltage. This totally eliminates leakage paths across the insulation package, as well as providing an interference shield and reducing common-mode capacitance. Circular lands on the printed circuit board surrounding the amplifier input terminal may also be connected to the guard voltage to minimize surface leakage currents. Figure 1.19(c) shows typical guarding connections for the unity-gain amplifier. Figure 1.21 shows typical guarding connections for the inverting and noninverting amplifier configurations.

Use of a Guard Terminal to Eliminate Common-Mode Signals

Grounded source, grounded voltmeter.   Figure 1.22 shows the most difficult measurement system, with both source and voltmeter grounded. Unwanted currents from external sources may flow between the source ground and the voltmeter ground, thus creating unwanted common-mode voltage V_{cm}. This causes unwanted common-mode current I_{cm} to divide between source resistances R_a and R_b. Because the voltmeter input impedance Z_1 is high, most of I_{cm} flows through R_b, which is in the measurement loop. Thus most of V_{cm} appears as a normal-mode voltage at the voltmeter input, and interference is large (Hewlett-Packard, 1986).